Fast Rail-to-Rail Operational Amplifiers Ease Design Constraints in Low Voltage High Speed Systems

by Eamon Nash

Movement towards lower power supply voltages is driven by the demand that systems consume less and less power coupled with the desire to reduce the number of power supply voltages in the system. Lowering power supply voltages and reducing the number of supplies has obvious advantages. One such advantage is to lower system power consumption. This has the additional benefit of saving space. Lowering overall power consumption has a residual benefit in that there may no longer be a need for cooling fans in the system.

However, as the traditional system power supply voltages of ±15 V and ±12 V give way to lower bipolar supplies of ±5 V and single supplies of +5 V and +3.3 V, it is necessary for circuit designers to understand that designing in this new environment is not simply a matter of finding components that are specified to operate at lower voltages. Not all design principles used in the past can be directly translated to a lower voltage environment.

Reducing the power supply voltage to a typical op amp has a number of effects. Obviously, the signal swings both at the input and output are reduced. The required headroom between signal and rail (typically 1 V to 2 V in conventional amplifiers), which is of lesser importance with power supplies of ±15 V, now drastically reduces the usable signal range. While this reduction does not normally increase noise levels in the system, signal-to-noise ratios will be degraded. Because the designer can no longer use techniques such as increasing power supply voltages and signal swings in order to "swamp" noise levels, greater attention must be paid to noise levels in the system.

Both bandwidth and slew rate decrease as power supplies drop. However, it should be noted that smaller signal swings need lower slew rates to maintain the same bandwidth. In choosing an operational amplifier, close study of the data sheet is essential. Data sheet specifications that list slew rate and bandwidth under

different power supply conditions (e.g., ±5 V, +5 V and +3 V), along with corresponding loading conditions, are useful and necessary here.

Rail-to-rail amplifiers are seen as a solution to the dilemma of decreasing power supply voltages. The term rail-to-rail, while not exactly defined, refers to devices whose inputs and/or outputs can swing close to both rails. This definition does not put an exact value on "close to both rails", nor does it specify the loading conditions under which rail-to-rail performance must be maintained. Rail-to-rail op amps are a subset of single-supply op amps which are devices that operate on a single rail. The inputs and outputs of a single-supply op amp may or may not be able to approach the rails. In order to work successfully with rail-to-rail and single-supply op amps, an basic understanding of some commonly used output stages is necessary.
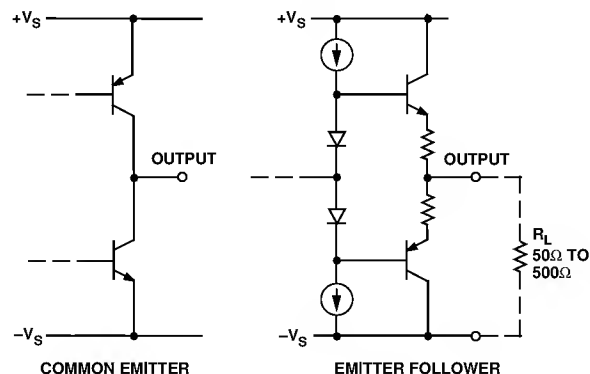

Figure 1. Common Op Amp Output Stages

Figure 1 shows two typical high speed op amp output stages. The emitter-follower stage is widely used in low distortion op amps. Its output voltage swing is limited to slightly greater than one diode drop from the rails. In reality, the headroom is closer to 1 V. In order to maintain low distortion at high frequencies, even more headroom may be required, reducing the available

peak-to-peak swing even further. Adding an external load resistor (typically 50 Ω to 500 Ω) referenced to the negative rail (this would be ground in a single-supply application) provides a pull-down path to the output. This, combined with the biasing on the bases of the NPN and PNP transistors, allows the PNP transistor to shut off. This allows the output to be pulled close to the negative rail so that the output stage behaves much like a simple NPN follower. This only allows the voltage to approach the negative rail. The load resistor would have to be referenced to the positive supply to bring the output voltage close to the positive rail. Another potential drawback of this configuration is the large load current that would be drawn for signal swings greater than a few hundred millivolts. Using a 50 Ω pull-down resistor, for example, would draw a current from the op amp of 40 mA if a 2 V p-p swing was desired.

The common-emitter stage shown allows the output to swing to within the transistor saturation voltage, V_{CESAT}, of both rails. For small amounts of load current (less than 100 µA), the saturation voltage may be as low as 5 mV to 20 mV; but for higher load currents, the saturation voltage may increase to several hundred millivolts (for example, 500 mV at 50 mA). This type of output stage has higher open-loop output impedance than an emitter follower stage and is more likely to distort when driving such nonlinear loads as flash converters. It is important though not to look at open loop output impedance in isolation. Closed loop output impedance, Z_o, is given by the formula

$$Z_o = \frac{Z_o}{1 + a_o \beta}$$

where Z_o is the open loop output impedance, a_o is the open loop gain and β is the feedback factor ($a_o\beta$ is commonly referred to as Loop Gain). So a large open loop gain, of 100 dB for example, would reduce the output impedance of an op amp, connected as a unity gain buffer, by a factor of 100,000. As frequency increases, the decreasing open loop gain will cause the output impedance to increase.

Even though rail-to-rail amplifiers can typically swing to within a few tens of millivolts of the power supplies, there is generally a tradeoff between distortion and signal swing. Data sheets of op amps usually specify optimum distortion with output signals that do not exercise the complete available voltage range. As signal levels approach within a few hundred millivolts of the rails, distortion performance degrades significantly. The best distortion/signal level tradeoff in rail-to-rail op amps, with common-emitter output stages, occurs when there is a signal-to-rail headroom of about 500 mV to each rail. This is a generalization and the optimal value will also depend on loading.

In addition to using rail-to-rail amplifiers, there are a number of techniques that can be used to increase signal swings without having to increase power supply levels. Differential drive circuits make more efficient use

of the available voltage range. Step-up transformers can increase voltages to an arbitrarily high level, but at the cost of increased output current from the driving amplifier. The following collection of common high speed applications seeks to illustrate the challenges involved in designing low voltage analog circuits and looks specifically at the techniques involved in obtaining optimal performance when using rail-to-rail op amps.

Driving High Speed ADCs
While most modern high speed ADCs operate from single supplies, they are still most often used in signal chains that have bipolar supplies. Because single-supply ADCs typically have lower quiescent currents than their dual supply equivalents, the main impetus behind this trend is the power that is saved.

Bipolar signals usually need some form of level shifting before being applied to a single-supply ADC. Because the safe input voltage to an ADC should not generally exceed the power supply voltages by more than a few hundred millivolts, consideration must be given to the protection of single-supply devices in a dual supply environment.

Figure 2 shows an 8-bit 125 MSPS flash converter being driven by a 240 MHz clamping amplifier. The ADC uses ECL logic and is powered from a single –5.2 V supply. The input voltage swing is 2 V (–1 V ± 1 V). The device's absolute maximum ratings specify a safe input voltage range to be between $-V_S$ and +0.5 V. While choosing a rail-to-rail amplifier to run from the same single supply would inherently protect the ADC from overvoltage, powering the op amp from a bipolar supply is more appropriate in this example.

Even though a rail-to-rail amplifier running on a single supply of –5.2 V would be capable of swinging most of the way up to ground, signal distortion tends to degrade significantly as voltages approach the rails. A more reasonable approach involves powering the op amp with bipolar supplies so that there is a large amount of headroom (5 V on the positive side and 3 V on the negative side) between the signal and the rails.

Using two resistor dividers, the input referred clamp voltages of the op amp are set to ±0.55 V or 50 mV greater than the normal maximum input voltages. In order to map the ±0.5 V input voltage into the 0 V to –2 V input range of the ADC, the op amp provides a gain of two and uses a +2.5 V reference to give a level shift of –1 V[1]. The output referred clamp voltages translate to +0.1 V and –2.1 V. The 1N5712 Schottky diode provides additional protection during power-up and actually holds the maximum voltage at the ADC's input to about +0.3 V. A 50 Ω resistor in series with the op amp's output limits the current through the diode during overvoltage as well as isolating the output stage from the signal dependent capacitive load of the flash ADC[2] that has a maximum value of 22 pF. The negative clamping level of –2.1 V, while not necessary to protect the converter, prevents excessive negative overdrive of the analog input.
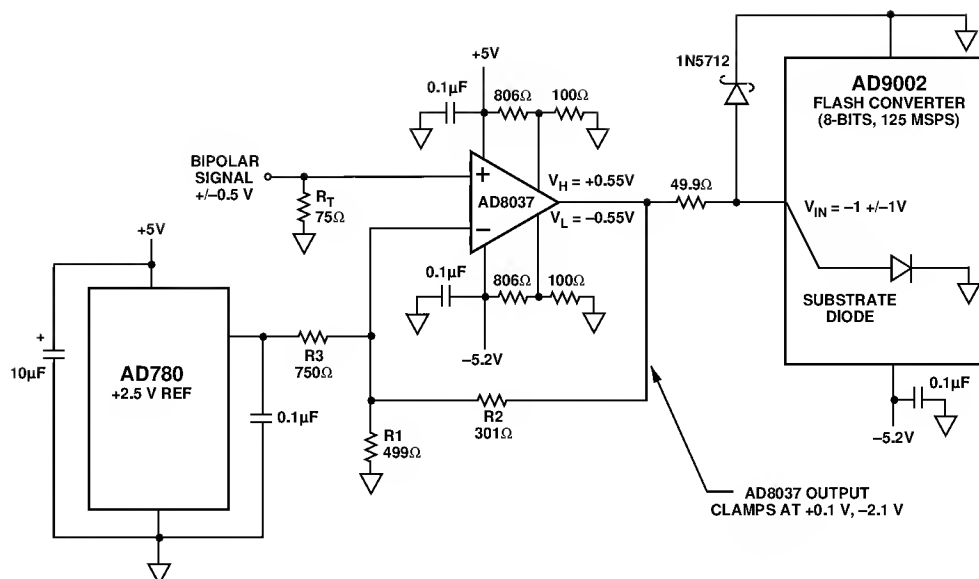
Figure 2. AD9002, 8-Bit, 125 MSPS Flash Converter

In addition to and perhaps more important than providing the necessary signal conditioning, a drive amplifier must provide a low impedance source which does not degrade the ADC's dynamic capabilities. The signal to noise plus distortion (S/(N+D) or SINAD) plot of the ADC should generally be used as the first selection criterion for the drive amplifier. This plot should be compared to the op amp's total harmonic distortion plus noise (THD+N). Comparing like with like is important here and both measurements should reference similar signal levels, power supply voltages and bias conditions as will be used in the actual circuit. The amplifier's loading conditions should also be similar to those presented by the ADC. As a general rule, in order to prevent the op amp from degrading the dynamic performance of the ADC, its THD+N should be 6 dB to 10 dB better than the ADC's S/(N+D) at the highest signal frequency[3] (usually but not always the ADC's Nyquist frequency). In some applications, such as spectral analysis, low distortion can be more important than low noise. In such cases, comparing the op amp's THD to the ADC's distortion (usually specified as spurious free dynamic range or SFDR) is more meaningful. Once again, choosing an op amp whose distortion is 6 dB to 10 dB better than the ADC's is appropriate.

This selection criterion can be used where the ADC's input impedance is fixed and does not change during the conversion process. This is usually the case with ADCs designed on bipolar processes. On the other hand, ADCs designed on CMOS processes typically connect the sample-and-hold switches directly to the analog input. This generates transient currents during the conversion that the external drive circuit must be able to deliver. In addition to this, the (relatively low) on-impedance of CMOS switches has some signal dependency. The ADC's analog input may, therefore, exhibit a signal-level-dependent input impedance, which leads to distortion.

Figure 3 shows a 12-bit 10 MSPS single-supply CMOS ADC being driven by a differential amplifier, created using a single-supply dual op amp. The input stage of the ADC is a differential sample-and-hold. The switches that open and close at the sampling frequency are shown in track mode. The capacitances denoted $C_{PAR}C_{PIN}$ are about 16 pF and represent the combined stray capacitance of the switches and the input pins. C_S and C_H represent the sampling and hold capacitances respectively. In the track mode, the differential input voltage is applied to the C_S capacitors. When it goes into hold mode, the voltages on these capacitors are transferred to the hold capacitors.

The input range of the ADC is set, by pin strapping, to 2 V peak-to-peak. The differential drive amplifier sets up a common-mode voltage of 2.5 V. From a signal distortion point of view, this is the optimal configuration for a number of reasons.

In systems that truly operate on a single power supply, it can often be difficult to maintain dc coupling from source all the way to the ADC. In such systems, a virtual ground is often created, usually centered halfway between the rails. This introduces the question of an optimum input voltage range for a single-supply ADC. At first glance, it would seem that a zero-volt referenced input might be desirable. But in fact, this places some severe constraints on both the ADC and its driving amplifier because both must maintain full linearity and low distortion at or near 0 V.

A more optimum voltage range for both ADC and op amp is one that includes neither ground nor the positive supply. A range centered around $V_S/2$ is usually optimum. For example, an input range of 2 V p-p centered around +2.5 V is bounded by +1.5 V and +3.5 V. If the dynamic specifications of single-supply op amps are stated for a midscale bias condition, a direct specification comparison can be made to help in making an

appropriate op amp ADC match. However, where a single-supply ADC has a bias point substantially offset from the ideal $V_S/2$, the op amp's distortion and other dynamic specifications may degrade.

In the example shown, the differential amplifier, which has a gain of two[4], converts a ±0.5 V single-ended signal to a 2 V peak-to-peak differential signal with a common-mode level of +2.5 V. Each of the op amps, however, is only required to swing from 2 V to 3 V (i.e., 2.5 V ± 0.5 V). This efficient use of signal range minimizes op amp distortion because of the relatively large headroom of 2 V to each rail. This scheme also has benefits for the converter. The on-resistance of the ADC's CMOS sampling switches, that was mentioned earlier, is at a minimum when the input voltage is at midsupply. Minimizing the voltage variation at each input decreases the signal dependent impedance variation of the switches and limits the resulting distortion.

This ADC can also be configured to accept an input voltage range, either single-ended or differential, of 5 V peak-to-peak. Using the configuration shown for a differential input range of 5 V peak-to-peak, the drive amplifiers would be required to swing from 1.25 V to 3.75 V. This still leaves 1.25 volts of headroom to both supplies. Choosing this larger input range optimizes dc linearity and signal-to-noise ratio. The increased signal range will cause a slight degradation in distortion in the converter.

From a safety point of view, the issue of clamping input voltages in a single-supply signal chain is of lesser importance because both amplifier and ADC are usually powered from the same source. However, the analog inputs on some ADCs have absolute maximum ratings that are less than the supply voltages. In these cases, the issue of input protection through clamping must once again be addressed.

Line Drivers
The Differential Gain and Differential Phase specifications are expressions of the variation of the gain and phase of a small signal as the magnitude of a large signal, on which it is superimposed, changes. While these specifications are primarily a function of amplifier architecture, the headroom between the signal and the power supplies will affect the differential gain and phase performance of an op amp. As a result, although composite video signals typically have maximum levels in the 1 V to 2 V range, composite video line drivers have, in the past, tended to run on power supplies of ±12 V and ±15 V. Systems designed nowadays require differential gain and phase specifications that are at least as good as those in the past. In order to save power, the designer can no longer afford the luxury of a large amount of headroom between signal and supplies.
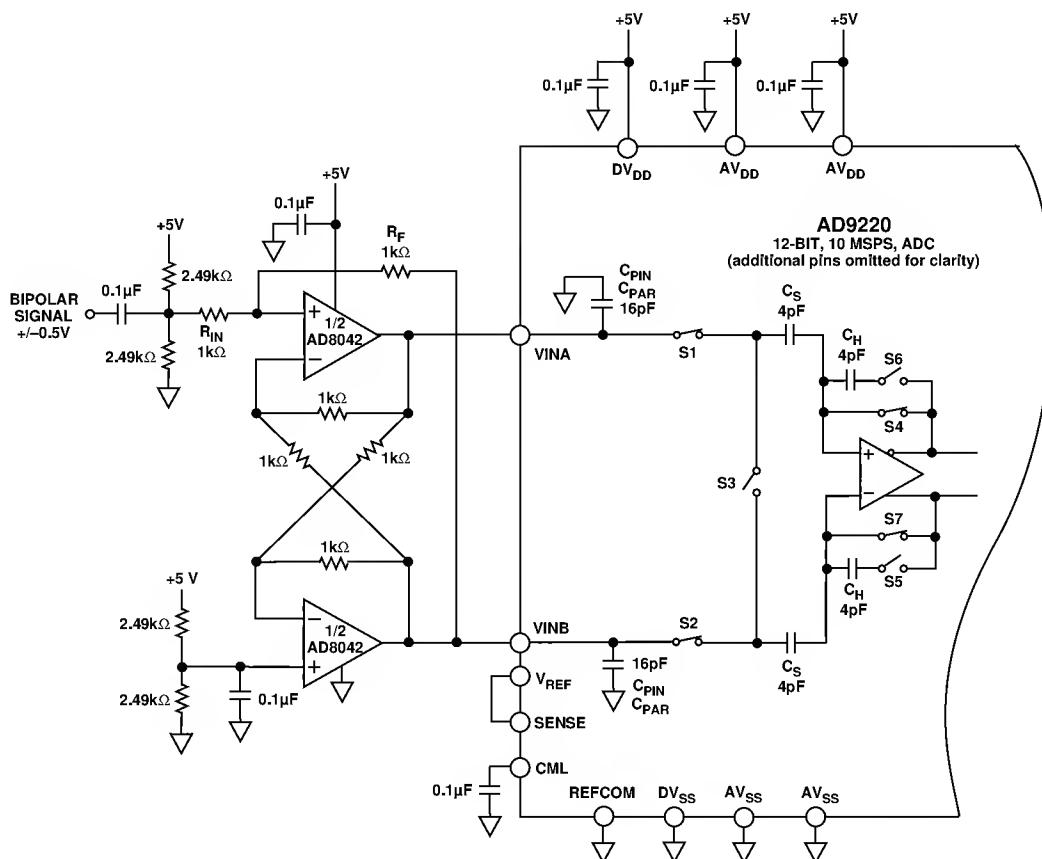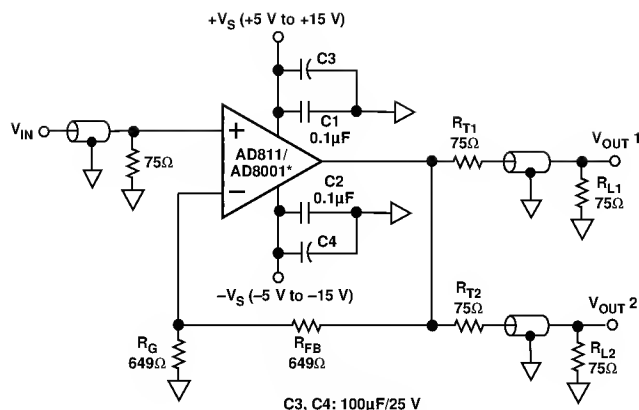

Figure 3. Driving a Single-Supply, Differential Input ADC with a Single-Ended to Differential Op Amp Configuration

*AD8001 CAN BE USED ONLY WHERE +/–5 V POWER SUPPLIES ARE PRESENT

Figure 4. Traditional High Quality Video Line Driver with Optional Video Distribution Function

Figure 4 shows a high performance video line driver, that has optional distribution amplifier features. The op amp stage operates at a gain of two, driving a pair of 75 Ω output lines through 75 Ω back terminations. V_{OUT1} and V_{OUT2} are thus individually isolated/buffered unity gain versions of V_{IN}. With the overall terminated gain of unity, this circuit serves well as a low distortion buffer, or a video distribution amp.

Exactly as shown, using the AD811 op amp and operated from ±15 V supplies, the circuit has a –3 dB bandwidth of 120 MHz, and differential gain/phase of 0.01%/0.01° with one line driven (R_L = 150 Ω). Driving two lines, the gain errors are essentially the same, while the phase errors rise to about 0.04°. The gain flatness of this circuit is within 0.1 dB to 35 MHz with ±15 V supplies. As expected, lower supplies do degrade performance some, but differential phase is still less than 0.18° with ±5 V power. The –3 dB point falls to 80 MHz, and 0.1 dB gain flatness is maintained to 25 MHz.

This example, which uses the AD811, illustrates the degree to which differential gain and phase degrade when power supplies are reduced from ±15 V to ±5 V. A more modern amplifier, like the AD8001 is only specified for operation at ±5 V. This amplifier has much higher bandwidth and 0.1 dB gain flatness and can almost equal the ±15 V differential gain and phase specifications of the AD811 and consumes less power.

For best accuracy and stability, the use of metal film resistor types is recommended. Heavy decoupling is also recommended. As a minimum, local low inductance/low ESR RF bypass caps should be used right at the device supply pins, shown as C1/C2. These are 0.1 µF surface mount chips (or other low inductance type). When driving high peak current loads, these high frequency bypasses should be augmented by local, short lead/large value, low ESR electrolytics, shown as C3/C4, in the range of 47 µF to 100 µF. These capacitors will carry the transient currents, and can be either tantalum, or aluminum types rated for high frequency (i.e., switching supply types).
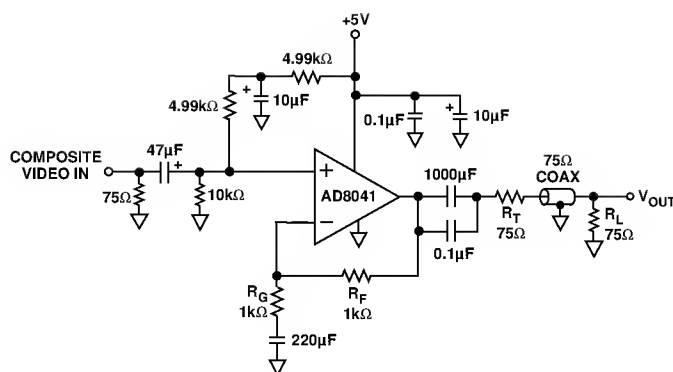

Figure 5. AC-Coupled Single-Supply Composite Video Line Driver

Figure 5 shows a schematic of a single-supply gain-of-two composite video line driver. Since the sync tips of a composite video signal extend below ground, the input must be ac-coupled and level-shifted positively. Setting the optimal bias point requires some understanding of the nature of composite video signals and the video performance of the op amp used.

After ac-coupling, signals of bounded peak-to-peak amplitude that vary in duty cycle, require larger dynamic swing capability than their peak-to-peak amplitude. As a worst case, the dynamic signal swing required will approach twice the peak-to-peak value. The two bounding cases are for a duty cycle that is mostly low, but occasionally goes high and vice versa. Composite video is not quite this demanding. One bounding extreme is a signal that is mostly black for an entire frame, but that has a white (full intensity) minimum width spike at least once per frame. The other extreme is for a video signal that is full white everywhere. The blanking intervals and sync tips of such a signal will have negative going excursions in compliance with composite video specifications. The combination of horizontal and vertical blanking intervals limit such a signal to being at its highest level (white) for only about 75% of the time.

As a result of the duty cycle variations between these two extremes, an ac-coupled 2 V p-p composite video signal requires about 3.2 V of dynamic voltage swing to avoid clipping.

Some circuits use a sync tip clamp along with ac-coupling to hold the sync tips at a relatively constant level in order to lower the amount of dynamic signal swing required. However, these circuits can have artifacts like sync tip compression unless they are driven by sources with very low output impedance.

Because the circuit shown uses an op amp with a rail-to-rail output stage, there is ample signal swing capability to handle the dynamic range required without using a sync tip clamp. As a test, the differential gain and phase were measured while the supplies were varied. As the lower supply is raised to approach the video signal, the first effect to be observed is that the sync tips become compressed before the differential gain and phase are adversely affected. As the upper supply is lowered to

approach the video signal, the differential gain and phase were not significantly adversely affected until the difference between the peak video output and the supply reached 0.6 V

Taking this test into account, it was found that the optimal point to bias the noninverting input was at 2.2 V dc. Operating at this point, the worst case differential gain and phase were measured at 0.06% and 0.06° respectively.

The ac-coupling capacitors used in the circuit appear quite large at first glance. A composite video signal has a lower frequency band edge of 30 Hz. The resistances at the various ac-coupling points, especially at the output, are quite small. In order to minimize phase shifts and baseline tilt, the large value capacitors are required. For video system performance that is not to be of the highest quality, the value of these capacitors can be reduced by a factor of up to five with only a slightly observable change in the picture quality.

A dc-coupled single-supply line driver presents a challenge if the voltage swing of output signal needs to go close to ground. This is because the signal distortion increases as the output voltage approaches ground. The AD8031 for example swings close to both rails. However lowest distortion performance is achieved when the signal has a common-mode level half way between the supplies and when there is about 500 mV of headroom to each rail. If low distortion is required in single-supply applications for signals which swing close to ground, an emitter follower circuit can be used at the op amp output.
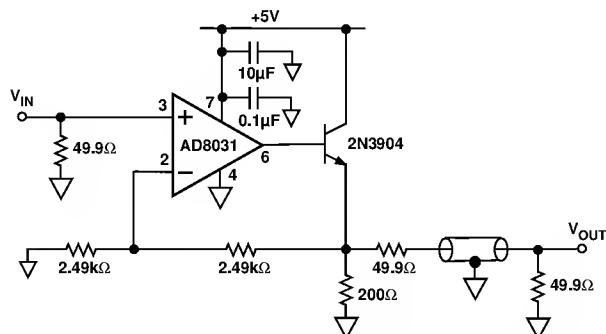

Figure 6. Low Distortion Line Driver for Single-Supply Ground Referenced Signals

Figure 6 shows the AD8031 configured as a dc-coupled single-supply gain-of-2 line driver. With the output driving a back terminated 50 Ω line, the overall gain from V_{IN} to V_{OUT} is unity. In addition to minimizing reflections, the 50 Ω back termination resistor protects the transistor from damage if the cable is short circuited. The emitter follower, which is inside the feedback loop, ensures that the output voltage from the AD8031 stays about 700 mV above ground. Using this circuit, very low distortion is attainable even when the output signal swings to within 50 mV of ground. The circuit was tested at 500 kHz and 2 MHz. Figures 7 and 8 show the output signal swing and frequency spectrum at 500 kHz. At this frequency, the output signal (at V_{OUT}), which has a peak-to-peak swing of 1.95 V (50 mV to 2 V), has a THD of –68 dB.
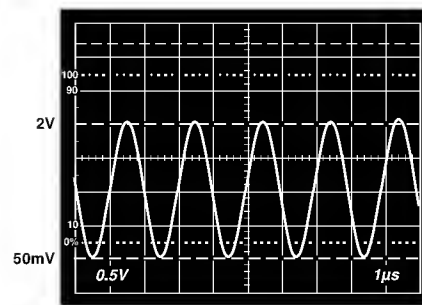

Figure 7. Output Signal Swing of Low Distortion Line Driver at 500 kHz
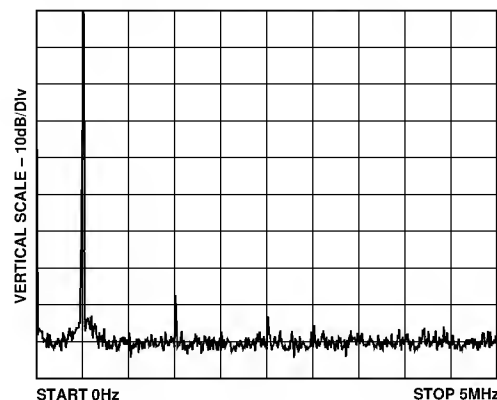

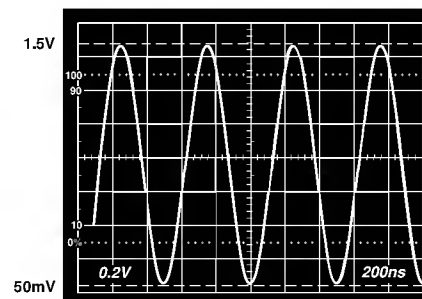Figure 8. THD of Low Distortion Line Driver at 500 kHz

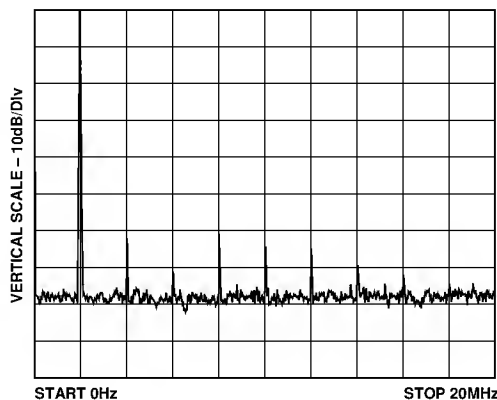Figure 9. Output Signal Swing of Low Distortion Line Driver at 2 MHz

Figure 10. THD of Low Distortion Line Driver at 2 MHz

Figures 9 and 10 show the output signal swing and frequency spectrum at 2 MHz. As expected, there is some degradation in signal quality at the higher frequency. When the output signal has a peak-to-peak swing of 1.45 V (swinging from 50 mV to 1.5 V), the THD is –55 dB.

This circuit could also be used to drive the analog input of a single-supply high speed ADC whose input voltage range is referenced to ground (e.g., 0 V to 2 V or 0 V to 4 V). In this case, a back termination resistor is not necessary (assuming a short physical distance from transistor to ADC). So the emitter of the external transistor would be connected directly to the ADC input. The available output voltage swing of the circuit would therefore be doubled.

Active Filters

Traditionally, when designing high speed active filters, a designer could choose an amplifier whose gain bandwidth product (GBP) was much higher than the corner frequencies of the filter. Additionally, a supply voltage of ±15 V or ±12 V meant that signal-to-rail headroom could be kept fairly large. This allowed the amplifier, from the point of view of bandwidth and signal swing at least, to be viewed as an ideal component. The advent of lower power supplies, which generally reduce bandwidth and slew rate, coupled with the desire to maximize signal range, means that in many cases, the difference between the corner frequency of the filter and the actual bandwidth of the amplifiers in the filter are no longer as far apart as before. In choosing an op amp for an active filter design, it is important to calculate beforehand, the bandwidth and phase shift that the amplifier will exhibit in the circuit, given the power supply levels, the desired signal swing and the required loading conditions. When considering signal swing, it is important also to consider the signal levels on the internal nodes of the circuit, not just the input and output levels. In filters with Qs over 0.707 there will be peaking in the response. The level of the peaking must be factored into the dynamic range of the filter so that no clipping occurs.

Many modern high speed op amps have a current feedback topology. Capacitance in the feedback loop of a current feedback amplifier usually causes it to become unstable. As a result, current feedback amplifiers are generally not usable in filter topologies that configure the op amp as an integrator[5]. An exception to this is the Sallen-Key filter which does not incorporate integrators.

Figure 11 shows a circuit for a single-supply biquad bandpass filter with a center frequency of 2 MHz. A 2.5 V bias level is easily created by connecting the noninverting inputs of all three op amps to a resistor divider consisting of two 1 kΩ resistors connected between +5 V and ground. This bias point is also decoupled to ground with a 0.1 μF capacitor. The frequency response of the filter is shown in Figure 12.

In order to maintain an accurate center frequency, it is essential that the op amp has sufficient loop gain at 2 MHz. This requires the choice of an op amp with a sig-

nificantly higher unity gain crossover frequency. The unity gain crossover frequency of the AD8031/AD8032 is 40 MHz. Multiplying the open-loop gain by the feedback factors of the individual op amp circuits yields the loop gain for each gain stage. From the feedback networks of the individual op amp circuits, we can see that each op amp has a loop gain of at least 21 dB. This level is high enough to ensure that the center frequency of the filter is not affected by the op amp's bandwidth. If, for example, an op amp with a gain bandwidth product of 10 MHz was chosen in this application, the resulting center frequency would shift by 20% to 1.6 MHz.
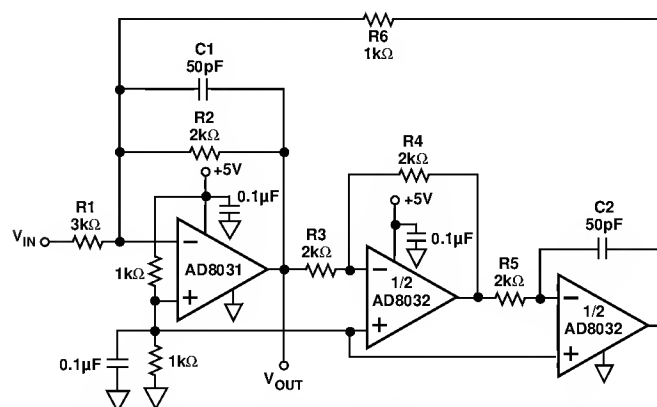

Figure 11. A Single-Supply 2 MHz Biquad Bandpass Filter Using AD8032 and AD8031
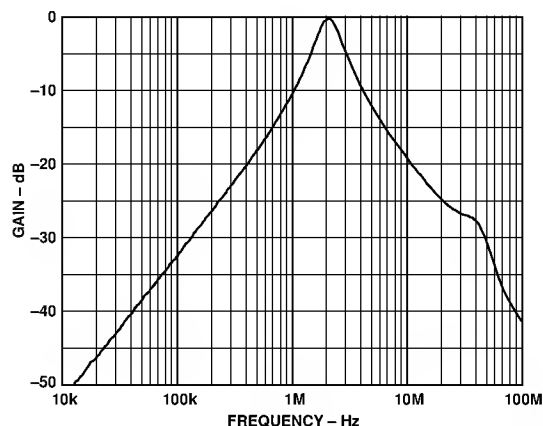

Figure 12. Frequency Response of Single-Supply 2 MHz Bandpass Filter

Transformer Drive Circuits

Even when using rail-to-rail amplifiers, an op amp's signal swing is limited to the power supply voltages. Using transformer coupling creates the possibility of increasing signal swings to voltages greater than the supply rails. Additionally, a transformer coupled signal, being differential, generally affords more immunity to external interference. This can be critical where signals are being transmitted over long distances.

The peak-to-peak amplitude of a signal can be increased to an arbitrarily high level by choosing a step-up transformer with the appropriate turns ratio. However, the reflected impedance from secondary to primary of a step-up transformer is equal to the secondary impedance divided by the square of the turns ratio. This leads

to a higher current demand on the op amp. In selecting a suitable op amp to drive a step-up transformer, the designer needs to look for good signal swing even when the amplifier is delivering relatively high current.

HDSL Transceiver

HDSL or high bit-rate digital subscriber line is becoming popular as a means of providing full duplex data communication at rates up to 2.048 Mbits/s over moderate distances via conventional telephone twisted pair wires. In order to achieve repeaterless transmission over distances of up to approximately 12,000 feet, a transmitted power level of +13.5 dBm (assuming a load impedance of 135 Ω) is required. Because the transceiver at the customer's end is sometimes powered via the twisted pair from a power source at the central office, circuit power consumption is critical.

Figure 13 shows a circuit powered from a single +5 V supply that can deliver this power level. A dual op amp is used to sum power into the two primary windings of the transformer. These are effectively connected in parallel. Both op amps are configured for a gain of 2. This allows the output to swing rail-to-rail even though the amplifier's input range is not rail-to-rail (input range is –0.2 V to +4 V). Although the output voltage is capable of swinging quite close to both rails even under fairly heavy loading conditions, a voltage swing from about 0.5 V to 4.2 V is more appropriate in order to maintain a THD level of about –70 dB (measured at 500 kHz). A 100 μF capacitor, to which both primary transformers are referenced, creates a virtual ground, equal to the average dc value of the output signal (about 2.4 V). Each primary has a reflected impedance from the secondary of 29.78 Ω (134/1.5²/2). The primaries are each connected in series with a resistance approximately equal to this value. So the voltage across each primary is half the voltage of the op amp driving it.
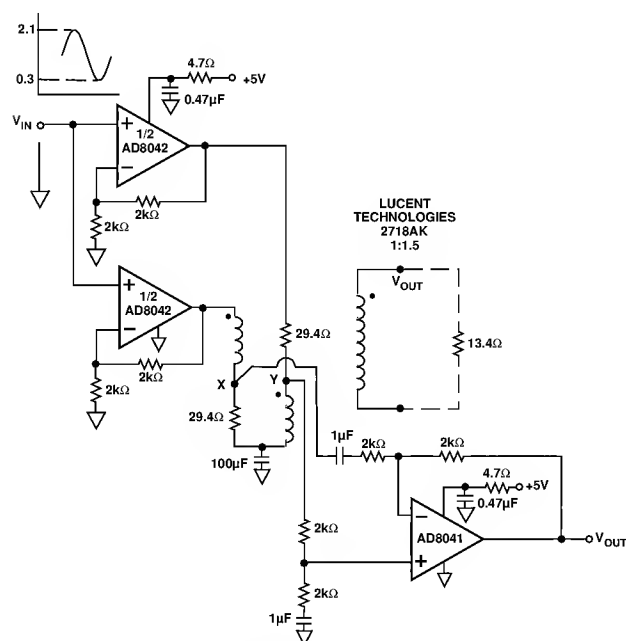

Figure 13. Single-Supply HDSL Transceiver

The divided down voltages from the two transmitter op amps are also fed to the two inputs of the differential receiver. These signals appear as a common-mode voltage to the receiver and are not amplified. In reality, the voltages at Nodes X and Y are not exactly equal, so some of the transmitted signal is amplified by the receiver. The transmitter to receiver rejection was measured at –20 dB.

The received signal couples on to both primaries. These voltages however drive the differential receiver 180° out of phase from each other. This results in a receiver gain which is equal to the inverse of the turns ratio of the transformer (1/1.5).

With each op amp delivering 3.5 V peak-to-peak at its output, each primary has a peak-to-peak voltage of 1.75. The secondary voltage of approximately 5.2 V peak-to-peak is the sum of the primary voltages times the turns ratio of 1.5. It corresponds to a power level of about +14 dBm. This is calculated using the equation.

$$Power = 10\,log_{10}\left[\frac{\left(\dfrac{V_{peak-peak}}{2 \times crest\ factor}\right)^2 / R_{LOAD}}{1\ mW}\right]$$

This power calculation is based upon a crest factor of $\sqrt{2}$. If a different crest factor is used in the calculation, the resulting power will be more or less than this value. If a higher signal swing is required, a transformer with a higher turns ratio can be used. This will demand more current from the op amps. In the configuration shown, the op amps are delivering about 28 mA to their loads which are referenced to +2.5 V. Because they are capable of delivering up to 50 mA while maintaining a signal swing of 0.5 V to 4.5 V, there is some scope for increasing the signal swing on the secondary. Increasing the turns ratio will, however, decrease the amplitude of the received signal.

References

1. *Replacing Output Clamping Op Amps with Input Clamping Amps*, Application Note AN-402, Analog Devices, 1995, p. 3

2. *Amplifier Applications Guide*, Analog Devices, 1992, pp. 7.49–52

3. *Practical Analog Design Techniques*, Analog Devices, 1995, pp. 4.12–15

4. *AD 8042, Dual 160 MHz Rail-to-Rail Amplifier*, Data Sheet, Analog Devices, 1995, pp 12-13

5. *Amplifier Applications Guide*, Analog Devices, 1992, pp. 6.27–29